

Attorney Docket No. 046006-272274
Appl. No. 10/087,450IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION of

LIANG et al.

Group Art Unit: 2819

Appln. No.: 10/087,450

Examiner: Unknown

Filed: February 28, 2002

FOR: FRAME RATE CONTROL SYSTEM AND METHOD

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October 25, 2002

PETITION TO MAKE SPECIAL UNDER
37 CFR §1.102(d) AND M.P.E.P. §708.02(VIII)

Hon. Commissioner of Patents
Washington, D.C. 20231

Sir:

Pursuant to 37 C.F.R. §1.102(d), and in accordance with the procedures set forth in M.P.E.P. §708.02(VIII), Applicants hereby petition to make the above-identified application special. The Petition fee as set forth in 37 C.F.R. §1.17(h) is enclosed herewith.

Applicants submit that the claims presented for examination are directed to a single invention. If it is determined that all the pending claims are not directed to a single invention, the Examiner is invited to telephone the undersigned; if necessary, Applicants will make an election without traverse as required under M.P.E.P. §708.02(VIII)(B).

Filed concurrently herewith is a Statement in support of the present Petition. The Statement specifies that a pre-examination search has been made; the scope of the search is

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set forth in the Statement. Further, the Statement contains a detailed discussion of the references deemed most closely related to the subject matter encompassed by the claims, which discussion points out, with the particularity required by 37 C.F.R. §1.111(b) and (c), how the claimed subject matter is patentable over the references.

Additionally, Applicants submit concurrently herewith: an Information Disclosure Statement; a Form PTO-1449 listing those references identified in the foregoing search; and a copy of each such reference.

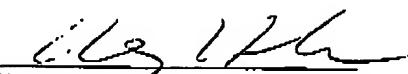
It is respectfully submitted that the present Petition, in conjunction with the attachments and enclosures identified above, is sufficient to comply with the requirements of 37 C.F.R. §1.102(d), and specifically, the provisions set forth in M.P.E.P. §708.02(VIII).

Accordingly, Applicants respectfully request that the present Petition be granted, and that examination of the present application be accelerated. Applicants request an early and favorable action on the merits.

Respectfully submitted,

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FOR: FRAME RATE CONTROL SYSTEM AND METHOD

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October 25, 2002

STATEMENT IN SUPPORT OF
PETITION TO MAKE SPECIAL UNDER
37 CFR §1.102(d) AND M.P.E.P. §708.02(VIII)

Hon. Commissioner of Patents
Washington, D.C. 20231

Sir:

Applicants respectfully submit the present Statement in support of the concurrently filed Petition To Make Special under 37 C.F.R. §1.102(d) and M.P.E.P. §708.02(VIII).

In accordance with M.P.E.P. §708.02(VIII)(A), the above-identified Petition and the appropriate fee as set forth in 37 C.F.R. §1.17(h) are filed concurrently herewith.

In accordance with M.P.E.P. §708.02(VIII)(B), Applicants submit that all the claims presented for examination are directed to a single invention. If it is determined that pending claims 1-43 are not directed to a single invention, the Examiner is invited to telephone the

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undersigned; if necessary, Applicants will make an election without traverse as required under M.P.E.P. §708.02(VIII)(B).

In accordance with M.P.E.P. §708.02(VIII)(C), Applicants hereby submit that a pre-examination search has been made. The scope of the search was as follows:

Class 345; Subclasses 660 & 698.

Additionally, Applicants submit concurrently herewith: an Information Disclosure Statement; a Form PTO-1449 listing the references identified in the foregoing search; and a copy of each such reference.

In accordance with M.P.E.P. §708.02(VIII)(E), following is a detailed discussion of the references deemed most closely related to the subject matter encompassed by the pending claims, which discussion points out, with the particularity required by 37 C.F.R. §1.111(b) and (c), how the claimed subject matter is patentable over the identified references.

Independent claim 1 recites a method of controlling a frame rate. The method includes comparing a write pointer and a read pointer. The method also includes, responsive to the comparing, adjusting a frequency of reading source data from a buffer. Independent claim 38 recites a computer readable medium encoded with instructions for such a method.

Independent claims 12 and 31 recite frame rate control systems. Each system includes a frequency controller configured to determine a relation between a value of a write pointer and a value of a read pointer and to indicate a reading frequency based on the determined relation.

Independent claim 21 recites a method of controlling a frame rate of a display signal. The method includes comparing information related to a write pointer and information related

to a read pointer. The method also includes, responsive to the comparing, detecting one of a buffer overflow condition and a buffer underflow condition and, responsive to the detecting, adjusting a display frequency in accordance with the detected condition.

Independent claim 44 recites a method of video signal processing. In this method, a frequency of a display signal is based on an amount of video data that has not yet been read from a buffer.

Each of the references 1)–6) discussed below mentions or suggests write and read pointers or addresses. However, none of these references discloses the elements of applicant's independent claims as set forth above. For example, none of these references discloses determining a relation between a write and a read pointer, and indicating a reading frequency based on the determined relation. Likewise, none of these references discloses a display signal having a frequency based on an amount of video data that has not yet been read from a buffer.

1) United States Patent No. 5,410,357 to Rieger et al. describes a scan converter. In this converter, an input horizontal synchronization rate is multiplied by a selected number of pixels per line to produce a WRITE pointer signal, and an output horizontal rate is multiplied by the selected number of pixels per line to produce a READ pointer signal (col. 1, l. 66 – col. 2, l. 4).

2) United States Patent No. 5,767,863 to Kimura describes a video processing technique using multi-buffer video memory. Specifically, a video memory is arranged as a

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buffer having four address groups. Video data may be read from and written into the same frame area as long as the read and write pointers do not overlap while accessing the same frame area (abstract). If the pointers are too close together, one of the pointers will not be allowed to enter that address group (abstract; col. 9, l. 10 – col. 10, l. 6).

United States Patent No. 5,568,165, also to Kimura, contains the same disclosure.

3) United States Patent No. 4,394,774 to Widergren et al. is directed to a digital video compression system. Specifically, this reference describes an adaptive coder that operates to keep a buffer as close to a half full position as possible (col. 8, l. 26 – col. 11, l. 10). To maintain buffer status, the coder codes input data according to a normalization factor, which factor is based on the number of bits loaded into a rate buffer memory during the last block or subframe (col. 19, ll. 5-11).

4) United States Patent No. 6,020,900 to Flurry, et al. describes a video capture method. The method includes determining when an actual amount of pixel data stored in a buffer reaches a set amount, and disabling further transfers to the buffer until pixel data already in the buffer is transferred to a data bus (col. 2, ll. 56-63; col. 3, ll. 4-12; col. 11, ll. 18-61).

5) United States Patent No. 6,078,361 to Reddy describes a video adapter circuit for conversion of an analog video signal to a digital display image. Data is read from a FIFO buffer into a video frame memory according to a read address pointer and a read clock. The read clock is generated by a VRAM clock, which is generated from an external oscillator

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operating at 50 MHz (col. 10, ll. 9-16). Data is read from a video frame memory to a flat panel display monitor according to a read address and control signals generated based upon values stored in a read lag register and a panel timing register. These registers are initialized by a microcontroller (col. 11, ll. 28-63).

6) United States Patent No. 6,219,023 to Kim describes a video signal converting apparatus with display mode conversion. Figure 4 of Kim shows that read pixel clock signal R_Dclk is a function of the input horizontal sync signal $Hsync$ or Hin and the number of pixel clocks per line $RPCN$ (see also col. 6, l. 1 - col. 9, l. 13).

As demonstrated above, none of the references 1)-6) discloses elements of applicant's claims such as determining a relation between a write and a read pointer, and indicating a reading frequency based on the determined relation; or a display signal having a frequency based on an amount of video data that has not yet been read from a buffer.

References 7)-11) discussed below also do not disclose at least those elements of applicant's independent claims as set forth above.

7) United States Patent No. 5,760,784 to Bullis et al. describes a system and method for pacing the rate of display of decompressed video data. Video data is decompressed in a coder/decoder and then scaled in a scaling device before being provided to a frame buffer. A buffer implemented within the scaling device may reach a threshold level whereby it is not desired that any more scaled data be received before being transmitted to the frame buffer.

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When such a threshold level is reached, a stall signal is sent to the interface between the scaler device and the coder/decoder, which results in the stopping of the transmission of pixel data from the coder/decoder to the scaler device (abstract; col. 4, ll. 57-66).

8) United States Patent No. 6,177,922 to Schiefer et al. describes a multi-scan video timing generator for format conversion. Specifically, this reference describes a method and apparatus for synchronizing a display timing generator to a video input signal. Such synchronization is performed according to a selected operating mode of a display synchronizer 410 (col. 14, l. 14-32) using lock event signals which occur once per video input frame (col. 13, ll. 45-47).

9) United States Patent No. 6,304,297 to Swan describes a method and apparatus for manipulating the display update rate of video signals. Specifically, this reference describes manipulating the display update rate of video signals by adding or deleting frames (col. 2, ll. 25-53).

10) United States Patent No. 6,353,459 to Yeh et al. describes a method and apparatus for conversion of video data. Converted video data is written into a buffer at a first rate and is read out of the buffer at a second rate. In order to avoid overflow and underflow conditions, a threshold value is determined. This threshold value is based on the video format being converted and is used to trigger a video driver to start reading data out of the buffer (see abstract; col. 2, ll. 50-61; col. 6, ll. 1-7).

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11) United States Patent No. 6,181,300 to Poon et al. describes a display format conversion circuit with resynchronization of multiple display screens. Specifically, this reference teaches varying a vertical or horizontal blanking time of a first display device (e.g. an LCD display) to correspond to a frame rate of another display device (e.g. a CRT display) (col. 1, ll. 17-21; col. 2, l. 45 – col. 3, l. 10).

Applicants respectfully submit that the foregoing references, whether considered individually or in combination, neither teach nor suggest the subject matter recited in pending claims 1-47.

It is respectfully submitted that the above-identified Petition, in conjunction with the foregoing discussion and the attachments and enclosures identified above, is sufficient to comply with the requirements of 37 C.F.R. §1.102(d), and specifically, the provisions set forth in M.P.E.P. §708.02(VIII).

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